This Listing of Claims will replace all prior versions or listings of claims in this application.

LISTING OF CLAIMS

1. (Currently Amended) A communication device, comprising:

a signal modulator/demodulator (modem) having a digital signal processor for effecting radio communications;

a shared memory connected to the modem; and

an application processor (AP) having a central processing unit and a first bus master controller for controlling via a first common bus a plurality of ~~external~~ external peripherals~~;~~ and a second bus master controller for controlling via a second common bus, ~~a~~ the shared memory connected to the ~~AP via the first common bus and connected to the~~ modem ~~via a second common bus~~,

wherein the first bus master controller controls the plurality of external peripherals by using a packet generator issuing a packetized command commonly receivable by the plurality of external peripherals over the first common bus, and wherein the packetized command includes a module device select signal for selecting one of the plurality of external peripherals.

2. (Canceled)

3. (Previously Presented) The device of claim 1, wherein the shared memory is an SDRAM.

4. (Currently Amended) The device of claim 1, wherein the plurality of external peripherals ~~include~~ includes at least one of an image capture module, and a display~~, and a flash memory~~.

5. (Canceled)

6. (Currently Amended) The device of claim 1, wherein the selected one of the plurality of external peripherals returns a signal to the first bus master controller to acknowledge receipt of the packetized command.

7. (Currently Amended) The device of claim 1, wherein the packetized command packet includes:

a read/write command directed to the shared memory shared by the modem and the AP.

8. (Currently Amended) The device of claim 7, wherein data read from the shared memory is sent to the AP via the second common bus with a strobe signal, and wherein the strobe signal is used for strobing the data read into a register in the second bus master controller.

9. (Currently Amended) The device of claim 3, wherein the SDRAM includes a plurality of data banks and an interface for interfacing the second bus master controller via the ~~first~~ second common bus.

10. (Previously Presented) The device of claim 3, wherein the shared memory includes a first protection circuit for receiving address data from the AP and a second protection circuit for receiving address data from the modem, each for generating a protect signal upon simultaneously receiving the same address from the modem and the AP, wherein the protect signal is generated to

halt memory access by one of the modem and the AP in order to prevent simultaneous access of the same memory cells.

11. (Currently Amended) A communication device, comprising:

a signal modulator/demodulator (modem) having a digital signal processor for effecting radio communications;

a shared memory connected to the modem; and

an application processor (AP) having a central processing unit and a first bus master controller for controlling via a first common bus ~~connected to~~ a plurality of external peripherals; and a second bus master controller for controlling via a second common bus the ~~a~~ shared memory connected to the ~~AP via the first common bus and connected to the~~ modem ~~via a second common bus~~,

~~wherein the bus master controller further controls a flash memory via the first common bus;~~

wherein the first bus master controller controls the plurality of external peripherals operatively connected to the first common bus by issuing a packetized command commonly receivable by the plurality of external peripherals over the first common bus, and

wherein the packetized command includes a module device select signal for selecting one of the plurality of external peripherals.

12. (Canceled)

13. (Previously Presented) The device of claim 11, wherein at least one peripheral of the plurality of external peripherals is an image capture module.

14. (Canceled)

15. (Currently Amended) The device of claim 11, wherein the selected one of the plurality of peripherals returns a signal over the first common bus to the first bus master controller in the AP to acknowledge receipt of the packetized command.

16. (Canceled)

17. (Currently Amended) The device of claim ~~16~~ 11, wherein data read from the shared memory is transmitted via the ~~first~~ second common bus to the second bus master controller in the AP with a strobe signal, and wherein the strobe signal is for strobing the data read into a register in the second bus master controller.

18. (Previously Presented) The device of claim 11, wherein the shared memory is an SDRAM.

19. (Previously Presented) The device of claim 18, wherein the SDRAM includes a plurality of data banks and an interface for interfacing .

20. (Previously Presented) The device of claim 18, wherein

the SDRAM includes a first protection circuit for receiving address data from the AP and a second protection circuit for receiving address data from the modem and for generating a protect signal upon simultaneously receiving the same address from the modem and the AP.

21. (Currently Amended) An application processor (AP), for use in a communication device, comprising:

a central processing unit for processing data received from a plurality of external peripherals and from a shared memory ; ~~and~~

a first bus master controller for controlling via a first common bus the plurality of external peripherals~~,~~; and

~~and~~ a second bus master controller for interfacing with ~~a~~ the shared memory via a second common bus, wherein the shared memory ~~that~~ is connected to a signal modulator/demodulator (modem) ~~via a second common bus~~,

wherein the first bus master controller controls the plurality of peripherals by issuing a packetized command commonly receivable by the plurality of external peripherals over the first common bus, and

wherein the packetized command includes a module device select signal used for selecting one of the plurality of external peripherals.

22. (Canceled)

23. (Previously Presented) The device of claim 21, wherein the shared memory is an SDRAM.

24. (Currently Amended) The device of claim 21, wherein the plurality of external peripherals additionally includes at least one of an image capture module~~,~~ and a display~~, and a flash memory~~.

25. (Canceled)

26. (Currently Amended) The deviee of claim 21, wherein the selected one of the plurality of external peripherals returns a signal to the first bus master controller over the first common bus to acknowledge receipt of the packetized eommand.

27. (Canceled)

28. (Currently Amended) The device of claim ~~27~~ 21, wherein the data read from the shared memory is sent over the ~~first~~ second common bus to the AP with a strobe signal, and wherein the strobe signal is used for strobing the read data into a register of the second bus master controller.

29. (Currently Amended) The device of claim 23, wherein the SDRAM includes a plurality of data banks and an interface for interfacing the second bus master controller.

30. (Currently Amended) The device of claim 23, wherein the SDRAM includes a first protection circuit for receiving address data from the AP over the ~~first~~ second common bus and a second protection circuit for receiving address data from the modem ~~over the second common bus~~ and for generating a protect signal upon simultaneous receipt of the same address from the AP and the modem.

31. (Currently Amended) An application processor (AP) for use in a communication device comprising:

a central processing unit for processing data received from a plurality of external peripherals over a first common bus and from a shared memory over a second common bus; and

a first bus master controller for controlling via the first common bus the plurality of external peripherals; and

~~and~~ a second bus master controller for interfacing via the second common bus with ~~a~~ the shared memory that is connected to a signal modulator/demodulator (modem) ~~via a second common bus~~,

wherein the first bus master controller controls the plurality of external peripherals by issuing a packetized command commonly receivable by the plurality of external peripherals over the first common bus, and

wherein the packetized command includes a module device select signal for selecting one of the plurality of external peripherals.

32. (Canceled)

33. (Previously Presented) The device of claim 31, wherein the shared memory is an SDRAM.

34. (Currently Amended) The device of claim 31, wherein the plurality of external peripherals ~~include~~ includes at least one of an image capture module, and a display~~, and a flash memory~~.

35. (Canceled)

36. (Currently Amended) The device of claim 31, wherein the selected one of the peripherals returns a signal over the first common bus to the first bus master controller to acknowledge receipt of the packetized command.

37. (Canceled)

38. (Currently Amended) The device of claim ~~37~~ 31, wherein the data read from the shared memory is sent to the AP over the ~~first~~ second common bus with a strobe signal, and wherein the strobe signal is used for strobing the data read into a register in the second bus master controller.

39. (Currently Amended) The device of claim 33, wherein the SDRAM includes a plurality of data banks and an interface for interfacing with the second bus master controller over the ~~first~~ second common bus.

40. (Currently Amended) A method of controlling a communication device having a signal modulator/demodulator (modem) for effecting radio communications, an application processor (AP) having a central processing unit, a first bus master controller, and a second bus master controller, and a shared memory, the method comprising:

controlling via a first common bus a plurality of external peripherals using the first bus master controller; and

interfacing with the modem via the shared memory and a second common bus using the second bus master controller,

wherein the step of controlling the plurality of external peripherals includes issuing a packetized command commonly receivable by the plurality of external peripherals over the first common bus, and

wherein the packetized command includes a module device select signal for selecting one of the plurality of external peripherals.

41. (Canceled)

42. (Previously Presented) The method of claim 40, wherein the shared memory is an SDRAM.

43. (Currently Amended) The method of claim 40, wherein the step of controlling includes controlling at least one of an image capture module, and a display~~, and a flash memory~~ included in the plurality of external peripherals.

44. (Canceled)

45. (Currently Amended) The method of claim 40, wherein the selected one of the plurality of external peripherals returns a signal to the first bus master controller over the first common bus to acknowledge receipt of the packetized command.

46. (Canceled)

47. (Currently Amended) The method of claim ~~46~~ 40, wherein data read from the shared memory is transmitted over the ~~first~~ second common bus to the AP with a strobe signal, and wherein the strobe signal is for strobing the data read into a register in the second bus master controller.

48. (Currently Amended) The method of claim 41, further including receiving address data from the AP over the ~~first~~ second common bus and from the modem ~~over the second common bus~~ at the shared memory and generating a protect signal upon simultaneously receiving the same address from the modem and the AP.

49. (Canceled)

50. (Canceled)